

# Fine Edge and Bevel Film Cut Accuracy by A Novel and High Precision Wafer Centering System

Fuping Chen<sup>1, 2, a\*</sup>, WeiZhang<sup>1</sup>, Fujin Jia<sup>2</sup>, Kaixuan Wu<sup>2</sup>, Wenjun Wang<sup>2</sup>, Xiaoyan Zhang<sup>2</sup>, David H. Wang<sup>2</sup>, Jian Wang<sup>2</sup>, Jane Wang<sup>2</sup>, Harry Han<sup>2</sup>, Sally-Ann Henry<sup>3</sup>, Shena Jia<sup>2</sup>

<sup>1</sup> Fudan University Room 313, microelectronics building, 220 Handan Road, Yangpu District, Pudong New District, Shanghai, China

<sup>2</sup> ACM Research (Shanghai), Inc.

<sup>3</sup> ACM Research Inc

<sup>a</sup>Email:fuping.chen@acmrcsh.com

**Keywords:** fine cut edge, bevel cleaning, a novel and high precision wafer centering system, cut accuracy, excellent cleaning capability

## Abstract

As more and more wafer dies are produced at the edge of the wafer, wafer edge cleaning and etching has become increasingly important in the manufacturing process of complex thin film laminated integrated circuits. If the edge cut accuracy is not well controlled, the effective removal of film and contaminants will not be achieved. In this paper, we propose a fine edge cut control process with a novel and high precision wafer centering method. A high precision wafer centering system for determining and correcting the position of a wafer on its chuck so as to ensure the uniformity of the width of the wafer edge etched. A fine edge cut profile is beneficial for subsequent film growth, and excellent cleaning capability can prevent buildup of flakes and defects on the bevel. All the above advantages contribute to the improvement of wafer edge yield in the future of chip manufacturing.

## Introduction

With the progress of technical nodes, devices are getting closer and closer to the edge of the wafer. Due to the complex interaction between film deposition, photolithography, etching, and chemical-mechanical polishing during the device manufacturing process, unstable film accumulation, metal contamination residue and etching damage occurs at the edge of the wafer. The weak adhesion between these films and the inherent stress of the ultra-thick dielectric film in the wafer edge region can lead to serious peeling defects, particle contamination, etc. The yield at the wafer edge has always been the lowest in any technology node as a result of the above problems. As more and more wafer dies are produced at the edge of the wafer, these issues become increasingly important in advanced technology nodes. There is an urgent need to add bevel cleaning process during manufacturing process to prevent buildup of flakes and defects. Therefore, wafer edge cleaning and etching has become increasingly important in the manufacturing process of complex thin film laminated chips [1-4]. Compared with dry etching, wet bevel etching has the advantages of high selection ratio of the underlying material, no plasma damage to the wafer, and simple equipment [5-6]. In the wet bevel cleaning process, various types of dielectric film, metal film, organic material film and particle pollutants on wafer edge can be removed by different chemical liquids to clean the wafer edge to avoid the impact on the subsequent process and improve the yield of chip manufacturing.

It was very difficult to control the uniformity of etching width on the wafer edge and bevel. If the edge cut accuracy is not well controlled, the effective removal of film and contaminants will not be achieved. In the bevel cleaning process, if the placement position of the wafer deviates on the vacuum

chuck, the centering of the wafer and the chuck cannot be effectively guaranteed, thus affecting the uniformity of the wafer edge etching width.

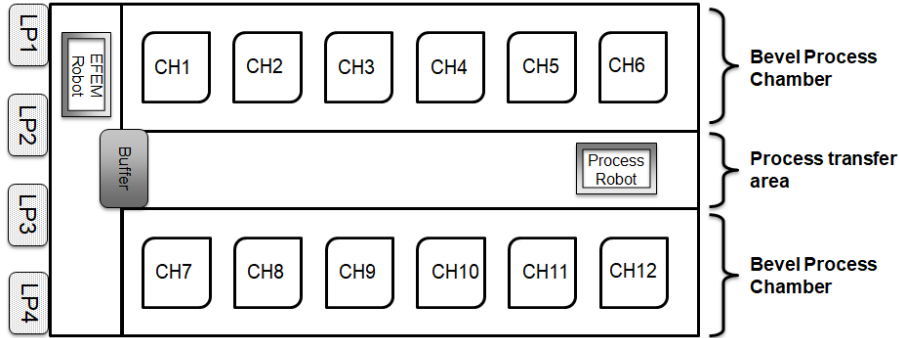


Figure 1: Simplified apparatus of Ultra C Bevel Cleaning System.

In this paper, we indicate a fine edge cut control process using ACM Ultra C Bevel tool, Fig 1, with a novel and high precision wafer centering method. A high precision wafer centering system for determining and correcting the position of a wafer on its chuck so as to ensure the uniformity of the width of the wafer edge etched. This wafer centering system not only has high precision, but also can be compatible with warped wafer, elliptical pieces, larger or smaller wafer ( $300\text{mm}\pm 0.5\text{mm}$ ) and other different situations.

## Experiment

To obtain fine edge and bevel film undercut, the process of wafer operation in the chamber is very important. Prior to wafer process, the wafer's position on the vacuum chuck needs to be verified and adjusted to ensure the concentricity of the wafer and chuck. As shown in Figure 2, figure 2A is a schematic diagram of our centering device. There are four contact points to ensure the accuracy of the wafer position when the wafer is centering, and R-Arm side has a displacement sensor. Firstly, we use 300mm standard diameter jig wafer to teach V(R) motor standard position  $P_{V1}(P_{R1})$ , and record the read value  $X1$  of the displacement sensor before it used for wafer centering. After the standard position is confirmed, we will take the test wafer to test, the whole centering process is as follow: a) V-Arm&R-Arm reaches the standard position  $P_{V1}/P_{R1}$ , if the displacement sensor reading  $X2$  is less than  $X1$ , this means the test wafer maybe larger than the standard 300mm. At this time, the wafer center is closer to R-Arm, V-Arm & R-Arm all need move to the V-Arm side  $(X2-X1)/2$ . On the contrary, V-Arm & R-Arm all need to move to the R-Arm side  $(X2-X1)/2$ . Now record the displacement sensor read value  $X3$ . b) V-Arm back to home position, R-Arm back to a safety position, VAC ON and wafer rotate  $180^\circ$ , R-Arm & V-Arm move to adjusted position just now, and record displacement sensor reading  $X4$ . c) If  $X3$  is less than  $X4$ , VAC OFF, V-Arm & R-Arm all need to move to the R-Arm side  $(X4-X3)/2$ . On the contrary, V-Arm & R-Arm all need to move to the V-Arm side  $(X4-X3)/2$ . d) VAC ON, real-time recording value of the displacement sensor when wafer rotates  $360^\circ$ . If the difference between the maximum and minimum values of the displacement sensor is less than  $0.05\text{mm}$  as shown in figure 2B, the centering ends and the wafer begins processing to achieve a fine edge cut control process, using ACM Ultra C Bevel tool with this novel and high precision wafer centering system.

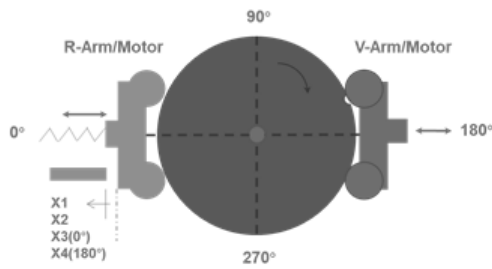


Figure 2A

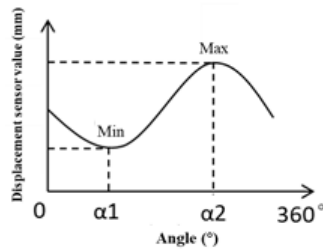


Figure 2B

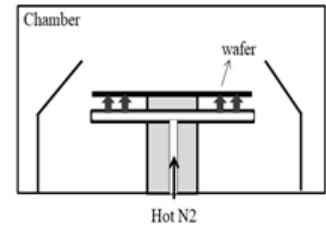


Figure 2C

Figure 2: Schematic diagram of wafer centering system (Figure 2A); Schematic diagram of displacement sensor readings (Figure 2B); Hot N2 heating wafer schematic diagram (Figure 2C)

## Results

Tests were carried out with the ACM Ultra C Bevel cleaning tool, 3 types of wafers and chemicals were used to show the capability of the tool.

- A Titanium Nitride (TiN) wafer was processed with SC1 (NH<sub>4</sub>OH, H<sub>2</sub>O<sub>2</sub>, H<sub>2</sub>O mixing) chemical mix ratio is set as 1:2:10 at room temperature, and wafer was heated by hot N<sub>2</sub> to reach the process temperature as shown in figure 2C.
- Thermal oxide / Aluminum (ThOx/Al) wafer processed with DHF (HF, H<sub>2</sub>O) chemical mix ratio of 1:10 at room temperature,
- ONON stack wafer was processed with 49%HF at room temperature, and wafer was heated by hot N<sub>2</sub> to reach the process temperature.

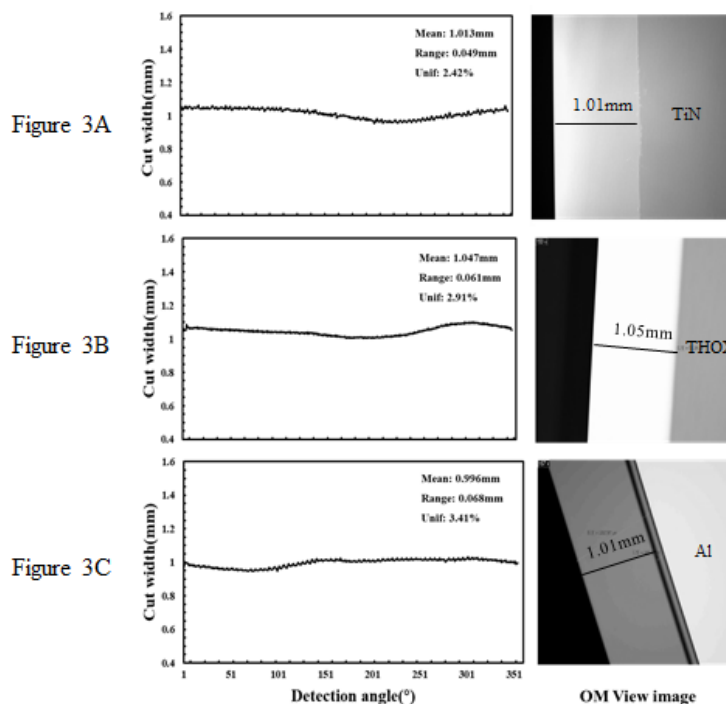


Figure 3: Different films undercut profile and edge cut image: TiN film (Figure 3A); THOX film (Figure 3B); Al film (Figure 3C)

Figure 3 shows different films bevel undercut profile and fine edge cut image after the bevel cleaning measured by the Wafer Edge Module (WEM) module in ACM Ultra C Bevel tool using high-precision centering system. As shown in Figure 3A, the boundary between the etched and non-etched areas on the TiN film wafer edge is very clear and smooth, this was processed with SC1+DIW Rinse + Spin Dry sequence. The bevel undercut width range (maximum-minimum) is only 0.049mm, which is a good uniformity 2.42%. As shown in Figure 3B, the boundary is also very clear and smooth between the etched and non-etched areas on the ThOx wafer edge which was processed with DHF+DIW Rinse+Spin Dry sequence. The ThOx wafer edge cut width range is only 0.061mm, and with a good uniformity 2.91%. As shown in Figure 3C, there is a gradient of 100um at the boundary between the etched and non-etched zones on the Al film wafer edge which was processed with DHF+DIW Rinse + Spin Dry sequence. The Al film wafer edge cut width range is only 0.068mm, with a good uniformity of 3.41%.

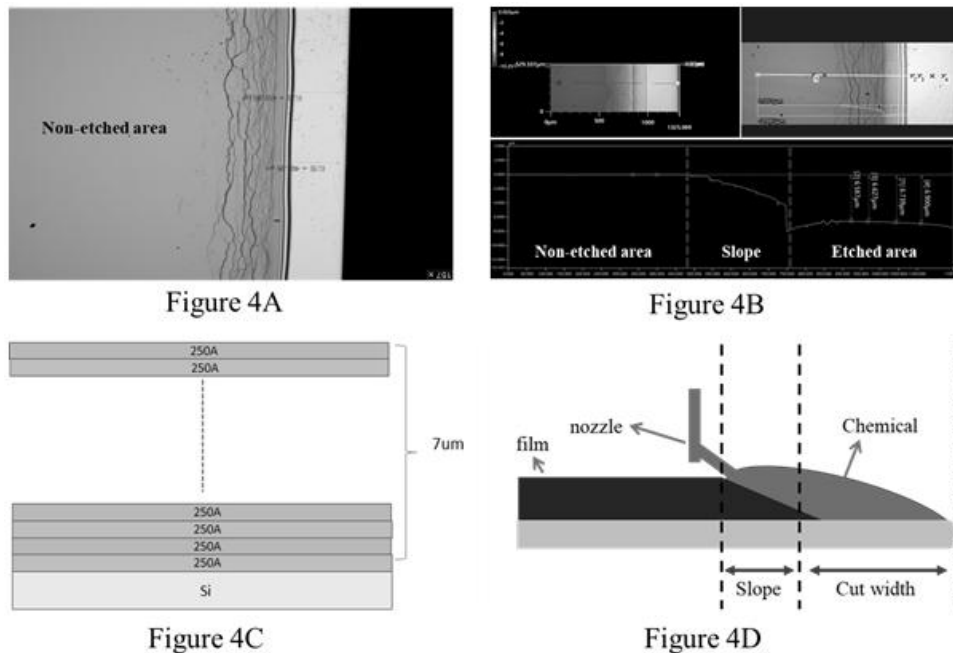


Figure 4: ONON film stack wafer edge cut profile: Edge cut image (Figure 4A); The film step height topography (Figure 4B); Schematic diagram of film stack (Figure 4C); Schematic diagram etching slope (Figure 4D)

As shown in Figure 4A, there is a gradient of over 400um at the boundary between the etched and non-etched zones on the ONON film stack wafer edge, which is due to thicker film thickness leading to a longer etching slope width. The result of the film step height topography is shown in Figure 4B and measured by an optical morphology measurement system. Figure 4C shows the structure of ONON stack film, which the total film thickness up to 7 microns. As shown in Figure 4D, we present a schematic diagram of the wafer edge cutting width affected by film thickness. This means that the thicker the film thickness is, the wider the slope width will be.

In the process of bevel etching process development of ONON film stack wafer, we found that ONON film cut width profile after bevel etching process would appear "half side effect". This means that one side of the wafer edge is well etched with no film residue, while the other side is poorly etched with more film residue remaining, as shown in the figure 5A. Through a series of experiments to verify, we finally deduced that there are two reasons for this phenomenon: One is that the temperature of the wafer is not high enough during the process; the second reason is that the temperature distribution of wafer edge is not uniform.

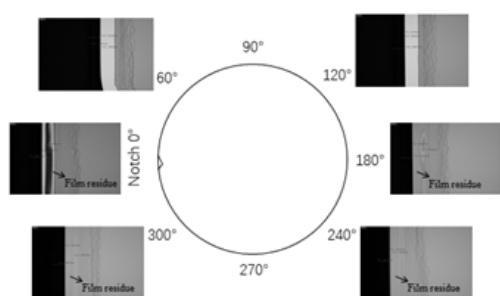


Figure 5A

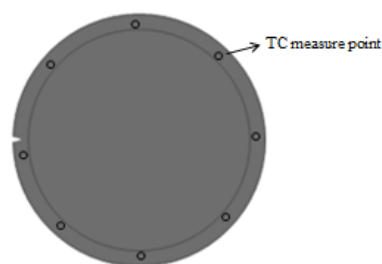


Figure 5B

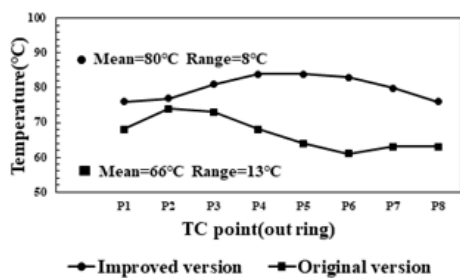


Figure 5C

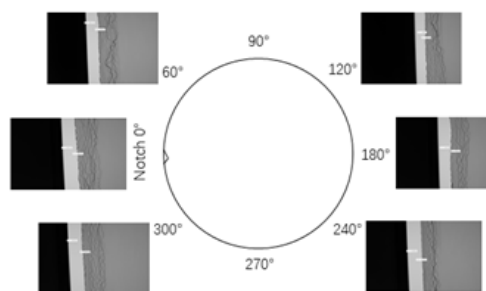


Figure 5D

Figure 5: ONON film stack wafer edge cut image with original version heating system (Figure 5A); Wafer edge thermometry tools diagram (Figure 5B); Wafer edge temperature data before and after heating system improvement (Figure 5C); ONON film stack wafer edge cut image with improved version heating system (Figure 5D)

To resolve this it, we upgraded the wafer heating module in our tool, including the heater and hot N2 channel, etc. As shown in the figure 5B, we use thermometry tools to measure the static temperature of several points on the edge of wafer. Compared with the original version, the wafer surface temperature of the improved version heating system is higher and more uniform as shown in the figure 5C. The improved heating system increased the heating efficiency by more than 20%, and the temperature range was reduced from the original 13°C to 8°C. As shown in the figure 5D, by keeping other process conditions remain unchanged, ONON film cut width with the improved heating system did not produce the "half side effect". Table 1 shows different angles of cut width of ONON film stack wafer with the two different kinds of heating system. The result shows that the improved version heating system not only has no "half side effect", but also has a very small cut width range, only 0.054mm.

Table 1 Different angles of cut width of ONON film stack wafer summary table with two different kinds of heating system.

Heating system	0° (mm)	60° (mm)	120° (mm)	180° (mm)	240° (mm)	300° (mm)	Range (mm)
Original version	Residue	0.326	0.318	Residue	Residue	Residue	0.326
Improved version	0.316	0.286	0.270	0.321	0.313	0.324	0.054

As shown in Figure 6, particle adder tests were processed in Ultra C Bevel tool with blanket wafers having a particle count <10ea@26nm and measured on a KLA-Tencor Surfscan SP3. This excellent bevel cleaning capability can prevent particles and defects on wafer edge and bevel be transferred to the device zone on the edge of the wafer.




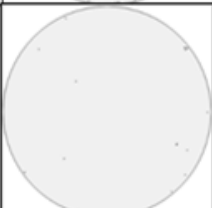


	Item	Sequence: SC1+DIW Rinse+Spin Dry		
		SLOT1	SLOT2	SLOT3
PA adder test	Pre			
	Post			
	Adding @26nm	5	9	1

Figure 6: Particle adding performance using Ultra C Bevel cleaning tool

## Conclusion

Over the ten last years, yield loss at the wafer edge has become more critical in advanced technology nodes as more and more dies are produced on the edge of the wafer. It is very necessary to insert a bevel cleaning process to prevent the particles and defects on the bevel be transferred to the device area close to the wafer edge. The optimization of bevel cleaning process to obtain fine edge and bevel film stripping has become increasingly important in the manufacturing process. In this study, a novel and high precision wafer centering system was proposed to obtain fine edge cut on the wafer edge. A fine edge cut profile is beneficial for subsequent film growth, and excellent cleaning capability can prevent buildup of flakes and defects on the bevel. All the above advantages contribute to the improvement of wafer edge yield in the future of chip manufacturing.

## References

- [1] Fine Edge and Bevel Film Stripping Process by Novel Wet Cleaning Tool beyond 45nm Node, edited by Yoshihiro Ogawa et al. 1-4244-1142-4/07 ©2007 IEEE.
- [2] Tsultrim Tharchin et al.: Yield Enhancement Due to Addition of Bevel Cleans at Middle of Line(MOL) Zone. UCPSS (2018).
- [3] Backside and bevel contamination removal, edited by Pascal Besson et al. UCPSS (2015), Solid State Phenomena Vol 219 (2015) pp 272-275.
- [4] Bevel Rinse Optimization for Reduced Edge Defectivity and Improved Edge Yield, edited by Mary Claire Silvestre et al. 978-1-5090-0270-2/16 ©2016 IEEE.
- [5] Cleaning Technology for Advanced Devices beyond 20 nm Node, edited by Yoshihiro Ogawa. UCPSS(2013), Solid State Phenomena Vol 195 (2013) pp 7-12.
- [6] Cleaning of wafer edge, bevel and back-side with a torus-shaped capacitively coupled plasma, edited by Buil Jeon et al. 0963-0252/02/040520+05 © 2002 IOP.