Uniformity Enhancement in 3D NAND Etch Processes via N_2 Bubbling Si_3N_4 Removal and Poly-Si Etch-Back

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Abstract

The push for increasingly large-capacity non-volatile data storage necessitates an improvement in NAND flash memory technology. It challenges high volume manufacturing (HVM) to incorporate more complicated three-dimensional structures, such as gate line and channel hole architectures, that have ever-increasing aspect ratios. Consequently, in advanced NAND flash memory manufacturing, the etch back of the polysilicon (poly-Si) film in channel holes and the selective removal of Si_3N_4/SiO_2 film stacks in the gate line, are two crucial processes that help determine device performance. However, as the specifications of wet etch processes evolve, these two key process steps suffer issues of poor etch uniformity and serious by-product regrowth. Herein, we present an advanced N_2 bubbling technology incorporated in an ACM Ultra C wet bench (WB) tool, that addresses these concerns. The performance of the poly-Si etch back and selective silicon nitride (SiN) removal steps on blanket film wafers (BW) both showed significant improvements, which were ultimately demonstrated on patterned wafer (PW).

Keywords: NAND flash memory manufacturing, gate line, channel hole, N_2 bubbling technique, etch uniformity, byproduct regrowth

1. Introduction

Since the 1980s, NAND flash memory technology has been utilized for large-capacity non-volatile data storage.[1–4] By virtue of its high random read/write speed and relatively low cost, NAND flash memory technology has been widely incorporated in solid state drives, servers and other long-term storage devices.[5–7] With the rapid development of 5G wireless communications, smartphones, tablets, smart vehicles etc., the need for enhanced NAND flash memory storage capacity is critical. In recent years, the evolution of the technology has extended from planar to three-dimensional (3D) architecture (3D NAND) and breaking through the limitation of the smallest effective

size of the memory cell.[8–12] In order to avoid a further decrease in the cell size on planar structures, 3D NAND flash memory technology uses high aspect ratio (A/R) gate line[13,14] and channel hole structures,[15,16] resulting in added challenges for the HVM process.

Within the region of SiN/SiO_2 film stacks (N-O) in the gate line, silicon dioxide (SiO_2) films act as dielectric layers while SiN films are used as sacrificial layers. A wet etch process is required to completely remove SiN after the dry-etch of the N-O sidewalls stack. During this process, hot phosphoric acid (HPA) is commonly used as the etchant, with etch selectivity between SiN and SiO_2 films, as well as etch uniformity between SiO_2 layers being topics of critical ongoing research. In particular, the low mass and heat transfer efficiency of the etchant on high A/R structures leads to diminished etch uniformity and SiO_2 regrowth especially in advanced 3D structures.[19,20]

Numerous studies on improving the etch selectivity of SiN/SiO_2 films through regulation of wet process parameters have appeared in recent years,[21,22] particularly in the development of specialty etch chemicals.[23,24] In general, the following two reactions dictate the wet etch process:

$$(1)\quad Si_3N_4(s) + H_2O + H_3PO_4 \rightarrow (NH_4)_3PO_4 + H_2SiO_3$$

$$(2)\quad SiO_2(s) + H_2O \rightleftharpoons H_2SiO_3$$

The silicic acid (H_2SiO_3) formed as by-product of the SiN etch can inhibit the reversible reaction of SiO_2 etch, resulting in high SiN/SiO_2 etch selectivity. With the excess accumulation of silicic acid comes the problem of SiO_2 regrowth and due to the relatively low concentration of reactants coupled with the low mass and heat transfer efficiency of the etchants, the etch rate of the SiO_2 regrowth formed is poor.

In the channel hole area, the poly-Si plays a critical role as the conductive material due to its ability to fill deep hole structures uniformly.[16] The grain size and step coverage (*S/C*) of the poly-Si film are key factors in device performance and control of these parameters are made more difficult by these deeper channel holes. The *S/C* is calculated by the ratio of the poly-Si film thicknesses at the bottom and top of the channel hole. During poly-Si film deposition, a controlled mixture of silane (SiH_4) and disilane (Si_2H_6) is chosen to increase the grain size of the poly-Si film, at the expense of film thickness and uniformity.[15] Thus, a wet etch process, using heated ammonium peroxide mixture (HAPM)[25] is used to improve the *S/C* of the poly-Si film. During the wet etch process, the uniformity of poly-Si film thickness must be precisely controlled, which is quite challenging due to the high A/R of the channel hole and the difficulty for etch chemicals to infiltrate deep channel holes, all related to the low mass and heat transfer efficiency in a confined environment.

In the case of wet batch tools, 50 wafers are generally arranged in an etch bath with an inter-wafer space of 5 mm, thereby inducing laminar flow of etchants between the wafers. This laminar flow restricts the mass and heat transfer impact of the reactants

and products. It has been reported previously that the introduction of nitrogen (N_2) gas bubbles of controlled size and frequency results in the transition of a laminar flow to a turbulent flow state, which further enhances the mass and heat transfer efficiency.[26,27] Some studies have also found that the gas bubbling technique also provides agitation in the liquid resulting in improved the mass and heat transfer process, as well as improving etch uniformity.[28,29] While it has been verified that the gas bubbling technique can regulate the macro flow-field distribution of the etchant solution, its influence on the mass and heat transfer processes in micro structures of the wafer surface, such as high AR gate line and channel holes, is in need of further validation.

In this paper, the N_2 bubbling technique is used in an ACM Ultra C WB tool to investigate the uniformity improvement of the poly-Si etch back process, and on the SiN film removal process used in 3D NAND manufacturing using both blanket film wafers (BW) and patterned wafers (PW).

2. Methods

The configuration of the ACM Ultra C WB tool is shown in Figure 1. The tool consists of an equipment front end module (EFEM), wet process module and additional support units. In general, wafers are introduced from the FOUP through the load port (LP) and EFEM to a transfer buffer via a series of wafer transfer robots (WTR). The wet process module consists of chuck cleaning (CHCL) unit, chemical baths, wafer baths, wafer dryer, and corresponding plumbing. In this study a DHF bath was used to etch the native oxide films from the wafer surfaces prior to processing. An APM mixture was used for post-process clean, and selective SiN/SiO_2 film removal was performed an HPA bath. The poly-Si etch was performed in HAPM bath. Three water baths, including an overfill (OF) bath, quick dump rinsing (QDR) bath, and hot QDR (HQDR) bath were used immediately after the corresponding chemical treatments. The N_2 bubbling technique was conducted in the HPA and HAPM etch bath, via an array of six N_2 bubbling tubes working together in parallel at the bottom of the tank. Each tube had about thirty, 0.15 mm diameter holes. The dryer utilized an ultra-low pressure drying technique (ULD), specific to the high AR structure.

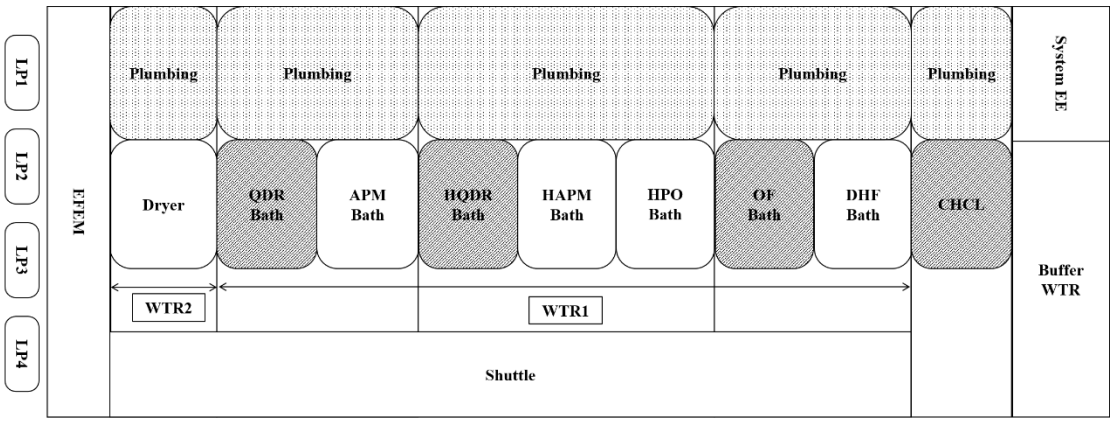


Figure 1. Simplified layout of ACM Ultra C WB tool

The blank wafers (BWs) used had 1000 Å SiN deposited by low pressure chemical vapor deposition (LP-SiN). Furthermore, two types of SiO_2 films were examined, consisting of 1000 Å thermal oxide (Th-OX) and 250 Å plasma enhanced chemical vapor deposition (PE-TEOS) oxide films. Similarly, 1000Å LPCVD poly-Si (LP-Si) films, which were deposited at 450℃ and 0.5torr, were studied.

3. Results and Discussion

3.1 Research of N_2 Bubbling in Silicon Nitride Removal Process

A comparison of the LP-SiN film etching process without/with N_2 bubbling is presented below. Table 1 shows the process conditions used for the film etch. Table 2 lists the flow rates used when N_2 bubbling is added to the etch solution.

Process	Condition (Conc. @Temp & Flow Rate)	Time (sec)
DHF	1:100 DHF @ 23°C & 20 L/min	30
OF (H_2O)	-	600
HPA	88.5% (w/w) @ 155.5°C & 29L/min	360
HQDR (H_2O)	-	600

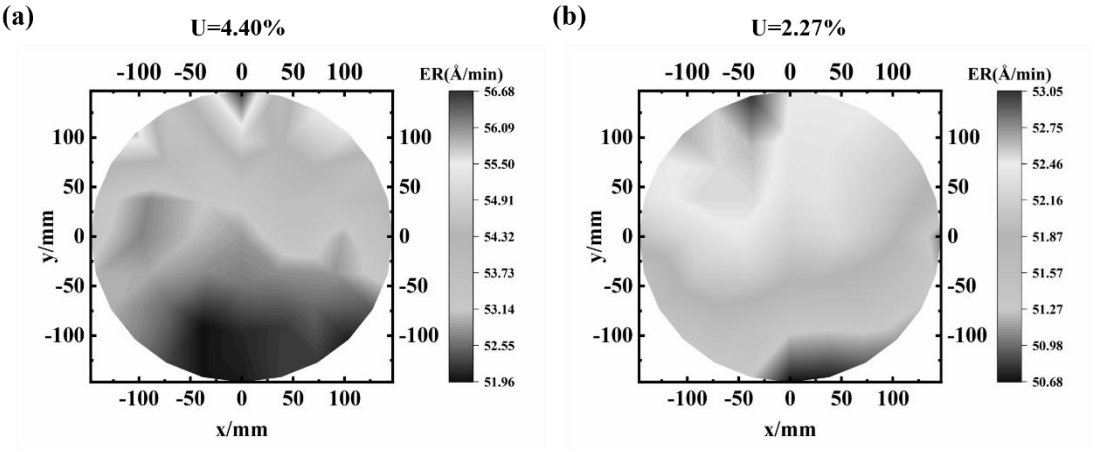
Table 1. Process sequence for SiN film removal with HPA for bubble tests.

Tube 1	Tube 2	Tube 3	Tube 4	Tube 5	Tube 6
1.2	0.8	0.8	0.8	0.8	1.2

Total flow = 5.6 L/min

Table 2. N_2 Bubble Generation Flow Rates (L/min) for HPA process

To simulate the conditions experiences in a 50 wafer boat a wafer is placed at the middle of the etch tank with a dummy wafer positioned on each side of it at a defined distance (≤ 5mm). This allows for control of the flow of liquid over the wafer and for an examination of the effect of that distance on the etch performance. A representative etch profile and corresponding etch rates (ER) within wafer, based upon ellipsometry†, is shown in Figure 2. The wafer was originally placed in the bath with the wafer notch at the top of the wafer and it is represented at coordinate (0, -150) in Figures 2a and b. Figure 2a highlights a significant variation in the etch rates across the wafer surface. There is preferential etching at the bottom of the wafer versus the top, consistent with the temperature and concentration variations in the etch bath likely due large-areal vortices and low thermal transfer efficiency in the bath. The calculated etch non-uniformity (*U*) is 4.34%. In Figure 2b, where N_2 is bubbled into the etchant mixture, the average ER drops by about 5% but *U* also decreased to 2.27%. There appears to be better etching, particularly through the wafer center, which is consistent with improved surface activity due to the addition of N_2 bubbling in the system.



†KLA-Tencor ASET-F5x ellipsometer

Figure 2. ER profiles of LP-SiN wafer by HPA solution (a) without N_2 bubbling (b) with N_2 bubbling

To investigate the relationship between (a) ER and different HPA temperatures and (b) different HPA concentrations, all with the presence of bubbling N_2, the following process flow used is shown in Table 3.

Process	Run	Condition (Conc._@Temp.& Flow Rate)	Time (sec)
DHF		1:100 DHF @ 23°C & 20 L/min	30
OF (H_2O)		-	600
HPA	1	88.5% (w/w) @ 155.5°C & 29L/min	360
	2	88.5% (w/w) @ 157.5°C & 29L/min	360
	3	88.5% (w/w) @ 159.5°C & 29L/min	360
	4	87.5% (w/w) @ 159.5°C & 29L/min	360
	5	88.5% (w/w) @ 159.5°C & 29L/min	360
	6	89.5% (w/w) @ 159.5°C & 29L/min	360
HQDR (H_2O)		-	600

Table 3. Etch matrix for HPA on LP-SiN and TH-OX varying temperature and concentrations.

Figure 3a shows the ERs of LP-SiN and TH-OX wafers at different temperature conditions, where the blue line represents the ER of LP-SiN and the red line refers to that of TH-OX. In both cases, the trend is for increased etch rate as a function of etchant temperature. The etch selectivity (*S*) however, decreased from 53 to 38 with increasing temperature. In Figure 3b the etch rate of LP-SiN decreases with etchant concentration as the etch rate of the TH-OX increases, but the *S* value also decrease from 39 to 33.

Thus, it can be concluded that the ER and *S* are more sensitive to variation of HPA temperature than concentration. In addition, there exists a trade-off relationship between the ER and *S* in response to the variation of HPA temperature.

Increased SiN/SiO_2 wet etch selectivity is the crucial parameter for advanced 3D NAND structure. Based upon the data observed the standard HPA process conditions lead to *S* values in the 40s, which falls short of the actual requirements for *S* to be around 700. Thus, novel HPA solutions with additives that can inhibit the SiO_2 etch are required. In one such test, 250 Å PE-TEOS was etched using a modified HPA solution, and the process time was increased to 30 min. The wafers were processed under two different conditions:

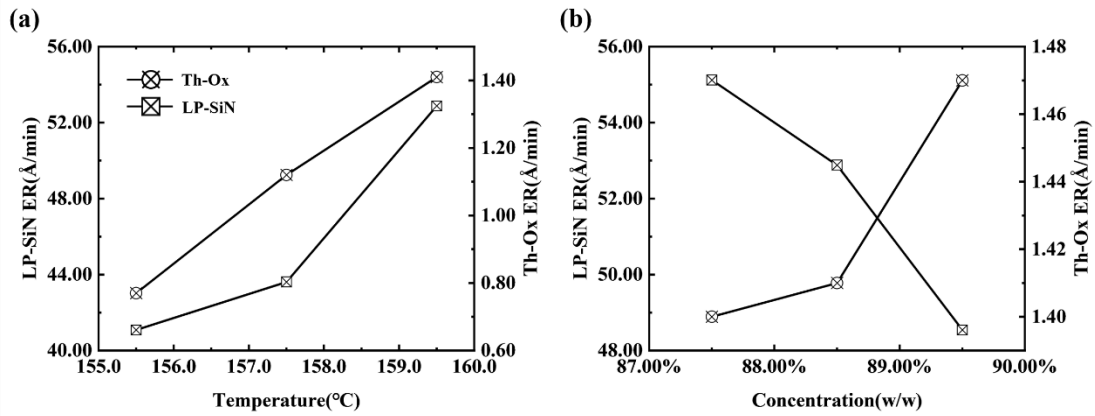


Figure 3. ERs of LP-SiN (blue line) and TH-OX (red line) wafers by HPA solution at different (a) temperatures and (b) concentrations

Process	Run	Condition (Conc. @Temp. & Flow Rate)	Time (sec)
DHF		1:100 DHF @ 23°C & 20 L/min	30
OF (H_2O)		-	600
HPA	1	88.0% (w/w) @ 158.5°C & 29L/min	1800
	2	88.5% (w/w) @ 159.5°C & 29L/min	1800
QDR (H_2O)		-	600
HAPM		1:2:50 APM* @ 35°C & 20 L/min	300
HQDR (H_2O)		-	

**29% w/w NH_4OH, 31% w/w H_2O_2*

Table 4. Etch matrix for HPA on LP-SiN and PE-TEOS varying temperature and concentrations.

The results of ER and *S* at two process conditions are given in Figure 4. While the etch rate for the LP-SiN behaves as expected, the etch rate for the PE-TEOS is significantly lower, and results in considerably enhanced *S* values of 899 and 657 respectively. While not yet optimized, this shows considerable promise in meeting the required specification.

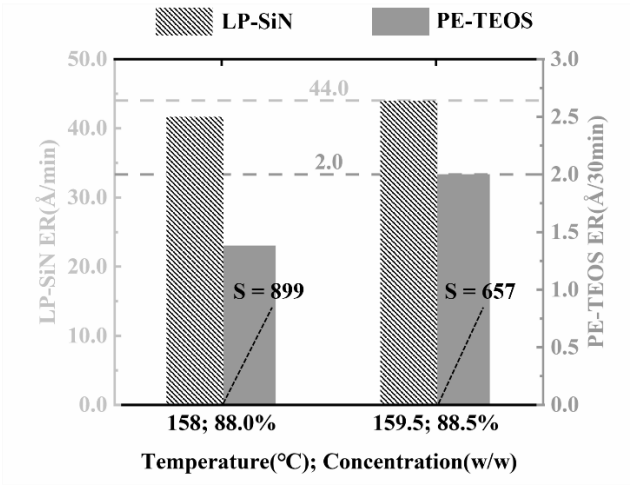
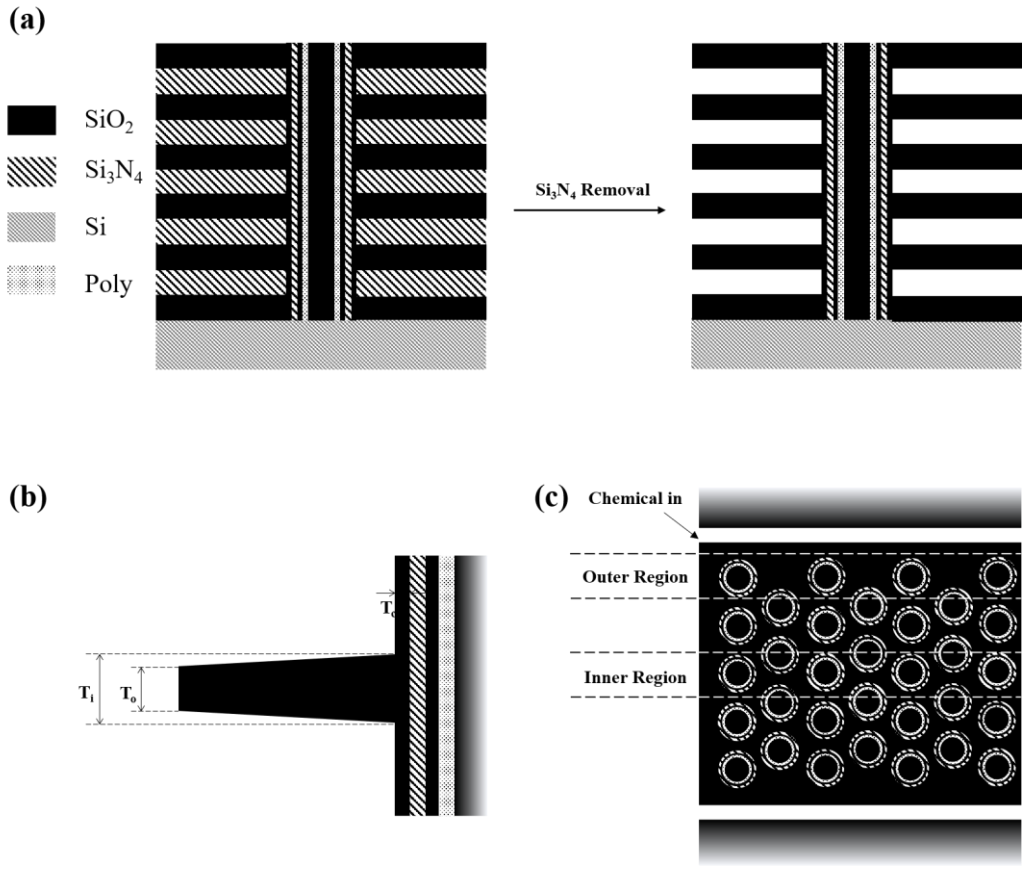


Figure 4. ER and S of LP-SiN and PE-TEOS wafers by special HPA at two different process conditions of temperature and concentration.

The work presented to this point was on blanket film wafers. In Figure 5a the results of the selective wet etch process of gate line N-O stacks on PWs without N_2 bubbling is reported. A HPA solution was used on SiN films in gate line N-O to completely remove the nitride film while selectively minimizing SiO_2 loss. The SiO_2 film that remained exhibited a defined trapezoidal shape where T_o and T_i represent the outer side and inner side, and the thicknesses are shown in Figure 5b. The T_o is supposed to be smaller than T_i, since the outer side will be exposed to special HPA longer when the SiN film is removed. This means there should be greater film loss at T_o than at T_i and both need to be thinner than the original etch. This precludes any SiO_2 regrowth. In the case of channel holes, the thickness of the SiO_2 film, T_c, should also be well controlled. Figure 5c shows a top-down view of one die, where the etch chemical enters stacked films from the trench of the die edge. Channel holes can be described as outer or inner region depending on their relative position to the die edge. Successful processing requires that thickness of all outer and inner channel holes (T_{oc} and T_{ic} respectively) are all in specification.

In HVM, the total number of N-O stacks layers is over 200 on the PW as provided*. To achieve complete removal of the SiN film stack, the process time was increased to 180 min (10800 sec). The SiO_2 film loss at the right and left edges of wafer were both measured and are listed in Table 5. The top layer film loss T_o limit was defined by the customer to be less ≤ 1.5 nm, and locations at the right and left edges of the PW were all found to be within specification. Furthermore, the film loss of T_o and T_i at the bottom of layers were positive values, which means the SiO_2 regrowth was avoided. The limit on SiO_2 film loss in the channel hole region is supposed to be ≤ 0.5 nm, with minimal thickness variation between T_{oc} and T_{ic}. Table 6 shows that this process met all the customer specifications above.

*Courtesy of Yangtze Memory Technologies Co. Ltd. (YMTC)



Wafers courtesy of Yangtze Memory Technologies Co. Ltd. (YMTC)

Figure 5. Schematic of (a) selective wet etch process of stacked SiN/SiO_2 films; SiO_2 film losses of (b) stacked layers and (c) channel holes on PW

Wafer Location	Layer Location	Film Loss of T_o (nm)†	Film Loss of T_i (nm)†
Edge/Right	Top	1.13	
	Bottom	0.6	0.28
Edge/Left	Top	1.29	
	Bottom	0.34	0.06

†*Determined by TEM*

Table 5. SiO_2 film loss at different locations of gate line N-O stacks on PW

Wafer Location	Layer Location	Film Loss of T_{oc} (nm) †	Film Loss of T_{ic} (nm) †
Edge/Right	Top	0.48	0.47
	Bottom	0.03	0.12
Edge/Left	Top	0.5	0.45
	Bottom	0.13	0.07

Table 6. SiO_2 film loss at different locations of channel holes on PW

3.2 Research of N_2 Bubbling in Poly-Si Etch Back Process

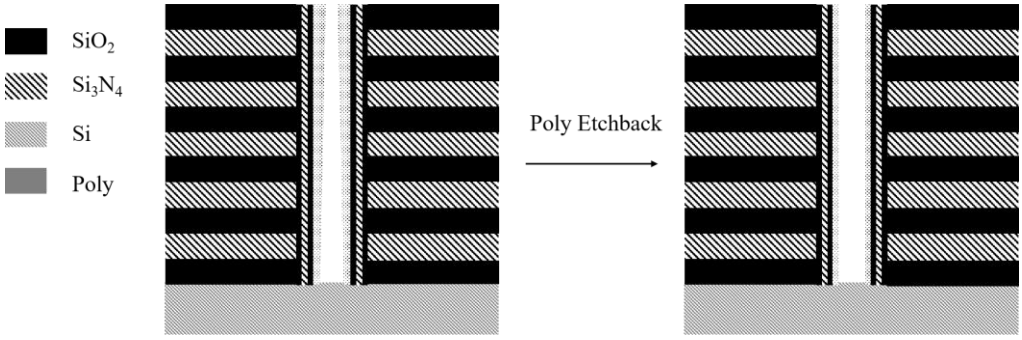


Figure 6. Schematic of etch back process of poly-Si film on the PW

The poly-Si etch back process on PW is represented in Figure 6. As previously mentioned, the LPCVD process results in more poly-Si being deposited at the top of the structure than at the bottom leading to the need for a wet etch back removal step. To optimize good *S/C*, the channel hole should have uniform poly-Si throughout. Given the results presented earlier concerning the positive impact of N_2 bubbling on etch uniformity, experiments were performed to look to further improve both the N_2 bubble process and the impact of overall APM flow on etch uniformity.

Table 7 outlines the parameters used to optimize the impact of N_2 bubble flow rate on the poly-Si etch uniformity on BW. In these tests the bubble flow rates were varied while the APM flow rate was held constant as described.

Run	Tube 1	Tube 2	Tube 3	Tube 4	Tube 5	Tube 6	Total N_2 flow
1	1.0	1.5	1.5	1.5	1.5	1.0	8 L/min
2	2.0	3.0	3.0	3.0	3.0	2.0	16 L/min
3	3.0	4.5	4.5	4.5	4.5	3.0	24 L/min

APM condition constant: 1:2:50 APM @ 70°C & 26 L/min

Table 7. Evaluation tests on the impact of N_2 bubble flow rates on poly-Si etch uniformity under constant APM condition

In Table 8 the conditions used to evaluate the impact of APM flow rate as a function of constant N_2 bubbling flow rate is described.

Process	Run	Condition (Conc. @Temp. & Flow Rate)	Time (sec)
HAPM	1	1:2:50 APM @ 70°C & 26 L/min	2400
	2	1:2:50 APM @ 70°C & 32 L/min	2400
	3	1:2:50 APM @ 70°C & 40 L/min	2400
HQDR (H_2O)		-	

Total N_2 bubble flow rate kept constant @ 16L/min

Table 8. Evaluation tests on the impact of HAPM flow rates on poly-Si etch uniformity under constant N_2 bubble generation conditions

The results of each test are presented in Figure 7. The etch non-uniformity shown in Figure 7a improved when the total N_2 bubble flow rate increased from 8 L/min to 16 L/min with the *U* value going from 1.53% to 1.04%. However, when the flow rate is increased to 24 L/min, *U* is diminished to a value of 1.46%. This would be consistent with there being a N_2 bubble flow rate "sweet" spot, either side of which leads to less etch uniformity. While it is generally accepted that higher chemical circulation flow rates results in the better etch performance in wet batch tools, the trend observed in Figure 7b again shows that the *U* value decreased indeed from 0.62% to 0.54% as the HAPM circulation flow changed from 26 L/min to 32 L/min, but rose to 1.04% when the APM circulation flow rate was increased to 40 L/min. It would also appear that there exists a trade-off between the total N_2 flow and HAPM circulation flow and that improved uniformity requires optimization of both.

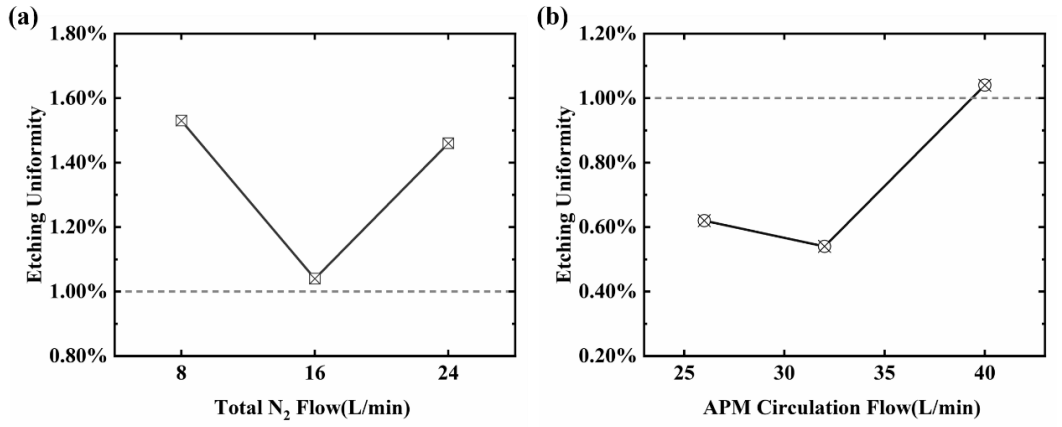
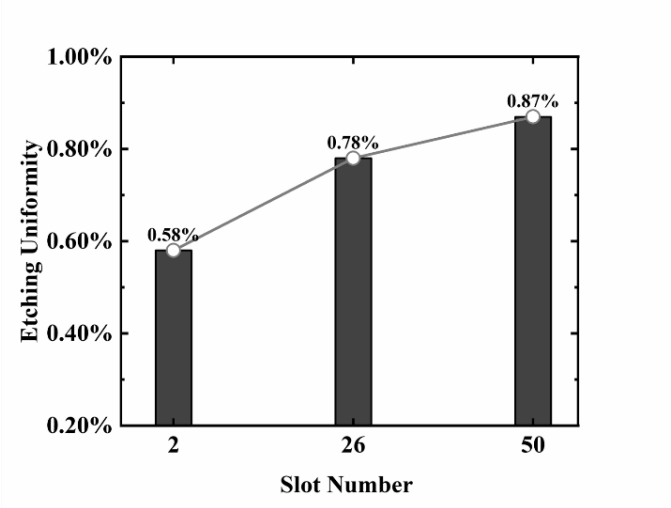


Figure 7. Effects of (a) N_2 flow or (b) HAPM flow on uniformity (*U*) of poly-Si film ER by HAPM solution. The dashed line represents the customer process performance specification.

Based upon the observations in Figure 7 the lowest *U* value appears when the N_2 bubble flow rate and APM circulation flow rate are 16 and 32 L/min respectfully. Utilizing these conditions the impact of slot position in the wafer boat was investigated to determine its impact on wafer-to-wafer (WTW) uniformity. Wafers were placed in

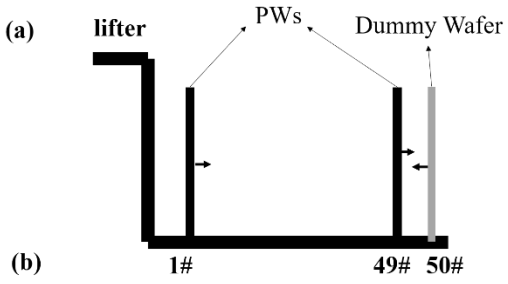
slots 2, 26 and 50 as representative positions across the etch tank. The *U* values were calculated as 0.58%, 0.78% and 0.87% respectively, and are shown in Figure 8. The rise in the non-uniformity of the wafers from slot 2 to 50 is attributed to a decrease in the horizontal velocity of the etchant and the relative decrease in N_2 bubble flow associated with the relative wafer positions in the tank. Despite these differences all wafer uniformities fall within the control limits set by the customer for these processes.



16 L/min N_2 bubble flow rate and 32 L/min APM circulation flow rate

Figure 8. The etch uniformity of wafers at slot 2, 26 and 50 under the optimum condition

Applying the same optimized conditions, the impact of wafer position on PWs was examined. High A/R channel holes structures, with a poly-Si film thickness of approximately 8 nm were utilized. The initial *S/C* of these wafers was around 90%. For the test, two PWs were located at slot 1 and 49 with one dummy wafer placed at slot 50, as seen in figure 9(a). The *S/C* and within wafer (WIW) etch uniformity after the wet etch process were measured and are shown in Figure 9(b). The results yielded S/C values of 118.6% and 117.3% for the biggest and smallest pitches, 240mm and 5mm, respectively. These values are within the target value range of 110% (±10%). Similarly, the WIW *U* values of 2.3% and 3.0% are consistent with the performance values in use for customer's HVM process.



Slot No.	S/C	U WIW
1	118.6%	2.3%
49	117.3%	3.0%

Figure 9. (a) Process slots of wafers on lifter; (b) The *S/C* and WIW uniformity of PWs at slot 1 and 49 under the optimum condition

4. Conclusions

It has been shown that the use of a selective wet etch process incorporating a N_2 bubbling technique in an ACM Ultra C WB tool results in enhanced SiN removal and poly-Si etch back process performances. The improvement in these processes is manifested in enhanced etch uniformity and diminished SiO_2 regrowth in gate line and high A/R channel hole structures. The N_2 bubble technique results in enhanced mass and heat transfer efficiencies of the etchants, and has been observed in both WIW and WTW performance. The relationship between ERs of LP-SiN/TH-OX films and process temperature or chemical concentration was demonstrated as was the trade-off between the N_2 bubbling flow and HAPM circulation flow in the poly-Si etch process. Both the WIW and WTW uniformities were optimized by regulating critical process parameters such as the N_2 flow and APM circulation flow. The ACM approach demonstrated on both BW and PW meet the requirements for HVM application.

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